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Attorneys for Plaintiff  
ALTAIR LOGIX LLC, a Texas limited liability company

**UNITED STATES DISTRICT COURT  
NORTHERN DISTRICT OF CALIFORNIA**

**ALTAIR LOGIX LLC,**

Plaintiff,

v.

**RENESAS ELECTRONICS AMERICA  
INC.,**

Defendant.

PATENT

Case No. \_\_\_\_\_

**ORIGINAL COMPLAINT FOR  
PATENT INFRINGEMENT  
AGAINST RENESAS  
ELECTRONICS AMERICA INC.**

**DEMAND FOR JURY TRIAL**

Plaintiff Altair Logix LLC files this Original Complaint for Patent Infringement against Renesas Electronics America Inc., and would respectfully show the Court as follows:

**I. THE PARTIES**

1. Plaintiff Altair Logix LLC (“Altair Logix” or “Plaintiff”) is a Texas limited liability company with its principal place of business at 15922 Eldorado Pkwy, Suite 500 #1513, Frisco, TX 75035.

2. On information and belief, Defendant Renesas Electronics America Inc. (“Defendant”) is a corporation organized and existing under the laws of California, with a place of business at 1001 Murphy Ranch Rd, Milpitas, CA 95035.

## II. JURISDICTION AND VENUE

3. This action arises under the patent laws of the United States, Title 35 of the United States Code. This Court has subject matter jurisdiction of such action under 28 U.S.C. §§ 1331 and 1338(a).

4. On information and belief, Defendant is subject to this Court's specific and general personal jurisdiction, pursuant to due process and the California Long-Arm Statute, due at least to its business in this forum, including at least a portion of the infringements alleged herein. Furthermore, Defendant is subject to this Court's specific and general personal jurisdiction because Defendant is a California corporation and it has a place of business within this District.

5. Without limitation, on information and belief, within this State and this District, Defendant has used the patented inventions thereby committing, and continuing to commit, acts of patent infringement alleged herein. In addition, on information and belief, Defendant has derived revenues from its infringing acts occurring within California and the Northern District of California. Further, on information and belief, Defendant is subject to the Court's general jurisdiction, including from regularly doing or soliciting business, engaging in other persistent courses of conduct, and deriving substantial revenue from goods and services provided to persons or entities in California and the Northern District of California. Further, on information and belief, Defendant is subject to the Court's personal jurisdiction at least due to its sale of products and/or services within California and the Northern District of California. Defendant has committed such purposeful acts and/or transactions in California and the Northern District of California such that it reasonably should know and expect that it could be haled into this Court as a consequence of such activity.

6. Venue is proper in this district under 28 U.S.C. § 1400(b). On information and belief, Defendant is incorporated in California, and it has a place of business within this District. On information and belief, from and within this District Defendant has committed at least a portion of the infringements at issue in this case.

7. For these reasons, personal jurisdiction exists and venue is proper in this Court under 28 U.S.C. § 1400(b).

**III. COUNT I**  
**(PATENT INFRINGEMENT OF UNITED STATES PATENT NO. 6,289,434)**

8. Plaintiff incorporates the above paragraphs herein by reference.

9. On September 11, 2001, United States Patent No. 6,289,434 (“the ‘434 Patent”) was duly and legally issued by the United States Patent and Trademark Office. The application leading to the ‘434 patent was filed on February 27, 1998. (Ex. A at cover).

10. The ‘434 Patent is titled “Apparatus and Method of Implementing Systems on Silicon Using Dynamic-Adaptive Run-Time Reconfigurable Circuits for Processing Multiple, Independent Data and Control Streams of Varying Rates.” A true and correct copy of the ‘434 Patent is attached hereto as Exhibit A and incorporated herein by reference.

11. Plaintiff is the assignee of all right, title and interest in the ‘434 patent, including all rights to enforce and prosecute actions for infringement and to collect damages for all relevant times against infringers of the ‘434 Patent. Accordingly, Plaintiff possesses the exclusive right and standing to prosecute the present action for infringement of the ‘434 Patent by Defendant.

12. The invention in the ‘434 Patent relates to the field of runtime reconfigurable dynamic-adaptive digital circuits which can implement a myriad of digital processing functions related to systems control, digital signal processing, communications, image processing, speech and voice recognition or synthesis, three-dimensional graphics rendering, and video processing.

1 (Ex. A at col. 1:32-38). The object of the invention is to provide a new method and apparatus for  
2 implementing systems on silicon or other chip material which will enable the user a means for  
3 achieving the performance of fixed-function implementations at a lower cost. (*Id.* at col. 2:64 –  
4 col. 3:1).

5  
6 13. The most common method of implementing various functions on an integrated  
7 circuit is by specifically designing the function or functions to be performed by placing on  
8 silicon an interconnected group of digital circuits in a non-modifiable manner (hard-wired or  
9 fixed function implementation). (*Id.* at col. 1:42-47). These circuits are designed to provide the  
10 fastest possible operation of the circuit in the least amount of silicon area. (*Id.* at col. 1:47-49).  
11 In general, these circuits are made up of an interconnection of various amounts of random-access  
12 memory and logic circuits. (*Id.* at col. 1:49-51). Complex systems on silicon are broken up into  
13 separate blocks and each block is designed separately to only perform the function that it was  
14 intended to do. (*Id.* at col. 1:51-54). Each block has to be individually tested and validated, and  
15 then the whole system has to be tested to make sure that the constituent parts work together. (*Id.*  
16 at col. 1:54-56). This process is becoming increasingly complex as we move into future  
17 generations of single-chip system implementations. (*Id.* at col. 1:57-59). Systems implemented  
18 in this way generally tend to be the highest performing systems since each block in the system  
19 has been individually tuned to provide the expected level of performance. (*Id.* at col. 1:59-62).  
20 This method of implementation may be the smallest (cheapest in terms of silicon area) method  
21 when compared to three other distinct ways of implementing such systems. (*Id.* at col. 1:62-65).  
22 Each of the other three have their problems and generally do not tend to be the most cost-  
23 effective solution. (*Id.* at col. 1:65-67).

24  
25 14. The first way is implemented in software using a microprocessor and associated  
26 computing system, which can be used to functionally implement any system. (*Id.* at col. 2:1-2).  
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28

1 However, such systems would not be able to deliver real-time performance in a cost-effective  
2 manner for the class of applications that was described above. (*Id.* at col. 2:3-5). Their use is  
3 best for modeling the subsequent hard-wired/fixed-function system before considerable design  
4 effort is put into the system design. (*Id.* at col. 2:5-8).

5  
6 15. The second way of implementing such systems is by using an ordinary digital  
7 signal processor (DSP). (*Id.* at col. 2:9-10). This class of computing machines is useful for real-  
8 time processing of certain speech, audio, video and image processing problems and in certain  
9 control functions. (*Id.* at col. 2:10-13). However, they are not cost-effective when it comes to  
10 performing certain real time tasks which do not have a high degree of parallelism in them or  
11 tasks that require multiple parallel threads of operation such as three-dimensional graphics. (*Id.*  
12 at col. 2:13-17).

13  
14 16. The third way of implementing such systems is by using field programmable gate  
15 arrays (FPGA). (*Id.* at col. 2:18-19). These devices are made up of a two-dimensional array of  
16 fine grained logic and storage elements which can be connected together in the field by  
17 downloading a configuration stream which essentially routes signals between these elements.  
18 (*Id.* at col. 2:19-23). This routing of the data is performed by pass-transistor logic. (*Id.* at col.  
19 2:24-25). FPGAs are by far the most flexible of the three methods mentioned. (*Id.* at col. 2:25-  
20 26). The problem with trying to implement complex real-time systems with FPGAs is that  
21 although there is a greater flexibility for optimizing the silicon usage in such devices, the  
22 designer has to trade it off for increase in cost and decrease in performance. (*Id.* at col. 2:26-30).  
23 The performance may (in some cases) be increased considerably at a significant cost, but still  
24 would not match the performance of hard-wired fixed function devices. (*Id.* at col. 2:30-33).  
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28

1           17.     These three ways do not reduce the cost or increase the performance over fixed-  
2 function systems. (*Id.* at col. 2:35-37). In terms of performance, fixed-function systems still  
3 outperform the three ways for the same cost. (*Id.* at col. 2:37-39).

4           18.     The three systems can theoretically reduce cost by removing redundancy from the  
5 system. (*Id.* at col. 2:40-41). Redundancy is removed by re-using computational blocks and  
6 memory. (*Id.* at col. 2:41-42). The only problem is that these systems themselves are  
7 increasingly complex, and therefore, their computational density when compared with fixed-  
8 function devices is very high. (*Id.* at col. 2:42-45).

10           19.     Most systems on silicon are built up of complex blocks of functions that have  
11 varying data bandwidth and computational requirements. (*Id.* at col. 2:46-48). As data and  
12 control information moves through the system, the processing bandwidth varies enormously.  
13 (*Id.* at col. 2:48-50). Regardless of the fact that the bandwidth varies, fixed-function systems  
14 have logic blocks that exhibit a “temporal redundancy” that can be exploited to drastically reduce  
15 the cost of the system. (*Id.* at col. 2:50-53). This is true, because in fixed function  
16 implementations all possible functional requirements of the necessary data processing must be  
17 implemented on the silicon regardless of the final application of the device or the nature of the  
18 data to be processed. (*Id.* at col. 2:53-57). Therefore, if a fixed function device must adaptively  
19 process data, then it must commit silicon resources to process all possible flavors of the data.  
20 (*Id.* at col. 2:58-60). Furthermore, state-variable storage in all fixed function systems are  
21 implemented using area inefficient storage elements such as latches and flip-flops. (*Id.* at col.  
22 2:60-63).

25           20.     The inventors therefore sought to provide a new apparatus for implementing  
26 systems on a chip that will enable the user to achieve performance of fixed-function  
27 implementation at a lower cost. (*Id.* at col. 2:64 – col. 3:1). The lower cost is achieved by  
28

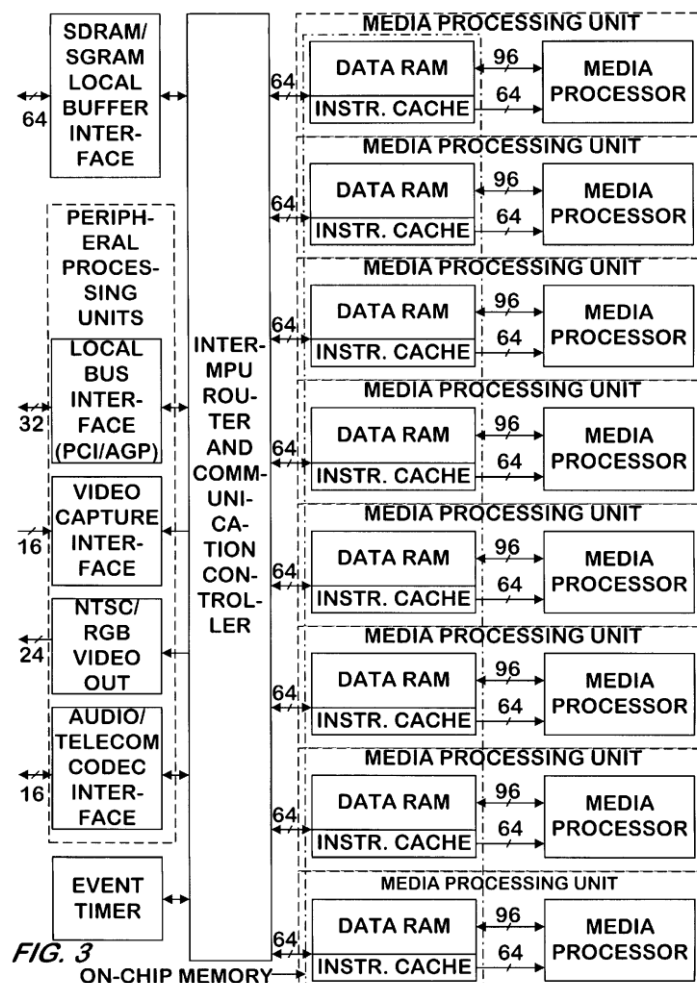
1 removing redundancy from the system. (*Id.* at col. 3:1-2). The redundancy is removed by re-  
2 using groups of computational and storage elements in different configurations. (*Id.* at col. 3:2-  
3 4). The cost is further reduced by employing only static or dynamic ram as a means for holding  
4 the state of the system. (*Id.* at col. 3:4-6). This invention provides a way for effectively adapting  
5 the configuration of the circuit to varying input data and processing requirements. (*Id.* at col. 3:6-  
6 8). All of this reconfiguration can take place dynamically in run-time without any degradation of  
7 performance over fixed-function implementations. (*Id.* at col. 3:8-11).

9         21. The present invention is therefore an apparatus for adaptively dynamically  
10 reconfiguring groups of computations and storage elements in run-time to process multiple  
11 separate streams of data and control at varying rates. (*Id.* at col. 3:14-18). The '434 patent refers  
12 to the aggregate of the dynamically reconfigurable computational and storage elements as a  
13 "media processing unit."

14         22. The claimed apparatus has addressable memory for storing data and a plurality of  
15 instructions that can be provided through a plurality of inputs/outputs that is couple to the  
16 input/output of a plurality of media processing units. (*Id.* at col. 55:21-30). The media  
17 processing unit comprises a multiplier, an arithmetic unit, and arithmetic logic unit and a bit  
18 manipulation unit. (*Id.* at col. 55:31 – col. 56:20). The '434 patent provides examples to explain  
19 each of the parts of the media processing unit. (*Id.* at col. 16:27-61 (multiplier and adder); *Id.* at  
20 col. 16:62 – col. 17:1-9 (arithmetic logic unit); and *Id.* at col. 17:10 – col. 17:43 (bit  
21 manipulation unit)). Each of the parts has a data input coupled to the media processing unit  
22 input/output, an instruction input coupled to the mediate processing unit input/output, and a data  
23 output coupled to the mediate processing unit input/output. (*Id.* at col. 55:31 – col. 56:20).  
24 Furthermore, the arithmetic logic unit must be capable of operating concurrently with either the  
25 multiplier or arithmetic unit. (*Id.* at col. 56:6-12). And the bit manipulation unit must be capable  
26  
27  
28

of operating concurrently with the arithmetic logic unit and at least either the multiplier or the arithmetic unit. (*Id.* at col. 56:13-20). Each of the plurality of media processing units must be capable of performing an operating simultaneously with the performance of other operations by other media processing units. (*Id.* at col. 56:21-24). An operation comprises the media processing unit receiving an instruction and data from memory, processing the data responsive to the instruction to produce a result, and providing the result to the media processor input/output. (*Id.* at col. 56:26-33).

23. An exemplary block diagram of the claimed systems is shown in Figure 3 of the '434 patent:





1 (*Id.* at Fig. 3). Exemplary architecture and coding for the apparatus is disclosed in the ‘599  
2 patent. (*E.g.*, *Id.* at col. 16:15 – col. 52:20; Figs. 9 – 106).

3 24. As further demonstrated by the prosecution history of the ‘434 patent, the claimed  
4 invention in the ‘434 patent was unconventional. Claim 1 of the ‘434 patent was an originally  
5 filed claim that issued without any amendment. There was no rejection in the prosecution  
6 history contending that claim 1 was anticipated by any prior art.  
7

8 25. A key element behind the invention is one of reconfigurability and reusability.  
9 (*Id.* at col. 13:26-27). Each apparatus is therefore made up of very high-speed core elements that  
10 on a pipelined basis can be configured to form a more complex function. (*Id.* at col. 13:27-30).  
11 This leads to a lower gate count, thereby giving a smaller die size and ultimately a lower cost.  
12 (*Id.* at col. 13:30-31). Since the apparatuses are virtually identical to each other, writing software  
13 becomes very easy. (*Id.* at col. 13:32-33). The RISC-like nature of each of the media processing  
14 units also allows for a consistent hardware platform for simple operating system and driver  
15 development. (*Id.* at col. 13:33-36). Any one of the media processing units can take on a  
16 supervisory role and act as a central controller if necessary. (*Id.* at col. 13:36-37). This can be  
17 very useful in set top applications where a controlling CPU may not be necessary, further  
18 reducing system cost. (*Id.* at col. 13:37-40). The claimed apparatus is therefore an  
19 unconventional way of implementing processors that can achieve the performance of fixed-  
20 function implementations at a lower cost. (*Id.* at col. 2:64 – col. 3:11).  
21

22 26. **Direct Infringement.** Upon information and belief, Defendant has been directly  
23 infringing claims of the ‘434 patent in California and the Northern District of California, and  
24 elsewhere in the United States, by making, using, selling, and/or offering for sale an apparatus  
25 for processing data for media processing that satisfies each and every limitation of at least claim  
26 1, including without limitation the EMMA EV2 multimedia processor (“Accused  
27  
28

Instrumentality”). (E.g.,

[https://www.renesas.com/us/en/doc/DocumentServer/030/r19ds0010ej1200\\_ds.pdf](https://www.renesas.com/us/en/doc/DocumentServer/030/r19ds0010ej1200_ds.pdf)).

27. The Accused Instrumentality comprises an addressable memory (e.g., memory system of the Accused Instrumentality) for storing the data, and a plurality of instructions, and having a plurality of input/outputs, each said input/output for providing and receiving at least one selected from the data and the instructions. As shown below, the Accused Instrumentality comprises a memory system which is coupled to multiple ARM processors through multiple internal inputs/outputs. The memory system provides instructions and stored data for processing and receives processed data.



Specifications in this document are subject to change.

## EMMA Mobile EV2 Data Sheet

R19DS0010EJ1200

Rev.12.00

Multimedia Processor for Mobile Applications

Jun 22, 2012

### DESCRIPTION



EMMA Mobile™ EV2 (EM/EV2) is an application processor for mobile multimedia handset devices. EM/EV2 utilizes two ARM® Cortex-A9 cores with two Neon extensions, an integrated audio video engine (AV engine), and a 3D graphics block to enable high-class processing in a range of applications. The processor contains a wide variety of interfaces for cameras, displays, mass storage devices, memory devices, and many other peripherals.

EM/EV2 achieves high-performance multimedia processing of up to HD-level decoding by means of hardware acceleration, while consuming minimal power..

(E.g., [https://www.renesas.com/us/en/doc/DocumentServer/030/r19ds0010ej1200\\_ds.pdf](https://www.renesas.com/us/en/doc/DocumentServer/030/r19ds0010ej1200_ds.pdf)).

**FEATURES**

- CPU: ARM Cortex-A9 (Frequency: 533 MHz, I-cache: 32 KB, D-cache: 32 KB, L2 cache : 256KB)
- AV engine: High-performance multimedia processor
  - Video:
    - Decoder: Multi decoder (H.264, VC-1, MPEG 1/2, H.263, MPEG-4: up to 1080p 30fps), other decoders/encoders may be implemented by software using CPU resources
  - Audio:
    - Decoder: MPEG-4 HE-AAC decoder, enhanced aacPlus decoder
- 3D Graphics accelerator (A3D)
  - 3D: 14.7 Mpix/sec
  - Supporting Open-GL-ES2.0, OpenGL-ES1.x
- Image processor: Resizing, rotating, image composing with alpha blending and key color masking
- Image composer: Image composing with alpha blending and key color masking, gamma correction
  - Direct connection to LCD interface
- Security functions: Secure boot function, secure timer, secure watchdog timer, secure DMA
- Internal memories: SRAM: 128 KB, ROM: 64 KB
- DMA controller: 8 channels
- Timers: Interval timers and watchdog timers: 15 channels
- DRAM interface:
  - LPDDR-SDRAM interface: Max 200 MHz DDR (DDR400), 32 bits, up to 1.6 GB/s
  - DDR2-SDRAM interface: Max 266 MHz DDR (DDR533), 32 bits, up to 2.1 GB/s
- NOR-Flash interface: 16-bit data bus
- Peripheral interfaces:
  - Memory card interface: SD card (with CPRM<sup>Note</sup>) × 1, SDIO × 3, CF card interface (Note : Option)
  - Image interfaces:
    - LCD interface → Parallel interface
    - ITU-R BT.656 interface
    - Camera interface → Parallel interface
  - Other serial interfaces:
    - USB 2.0 host × 1 and peripheral × 1 (with PHY)
    - UART × 4
    - I2C × 2
    - Unified serial interface × 6 (SPI, I2S)

(Id.).

28. The Accused Instrumentality comprises a plurality of media processing units (*e.g.*, multiple ARM cortex-A9 processors), each media processing unit having an input/output coupled to at least one of the addressable memory input/outputs. As shown below, the Accused Instrumentality comprises multiple ARM cortex-A9 processors, each processor comprises a NEON media coprocessor and acts as a media processing unit. The ARM processors are coupled to the memory system. The processors receive instructions and data from the memory system by multiple internal inputs and provide processed data to the memory system by multiple internal outputs.



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(Id.).

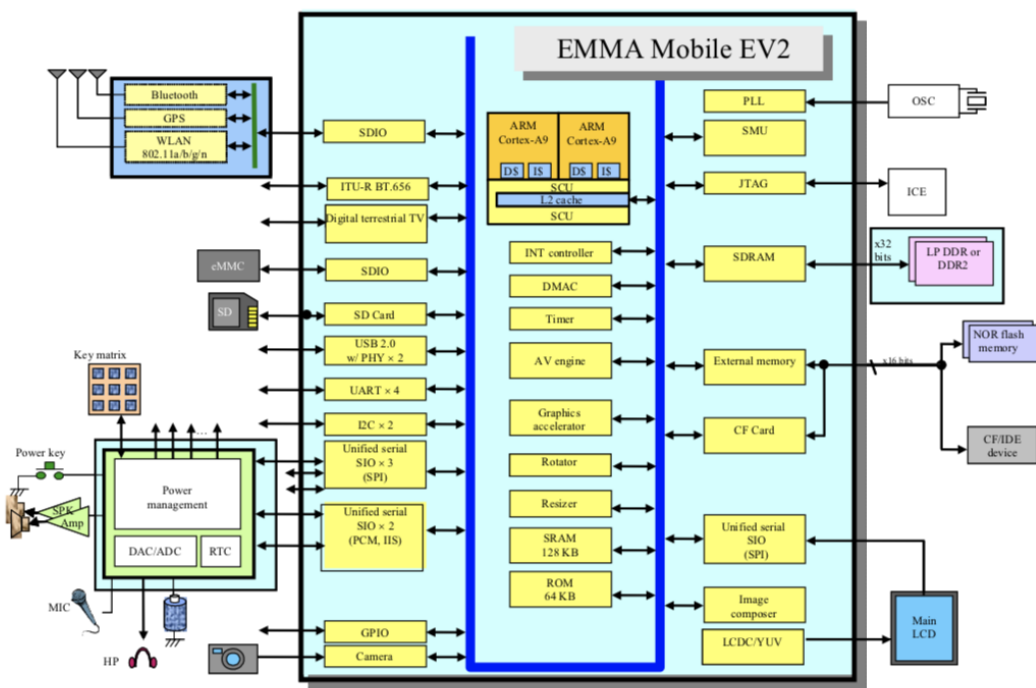
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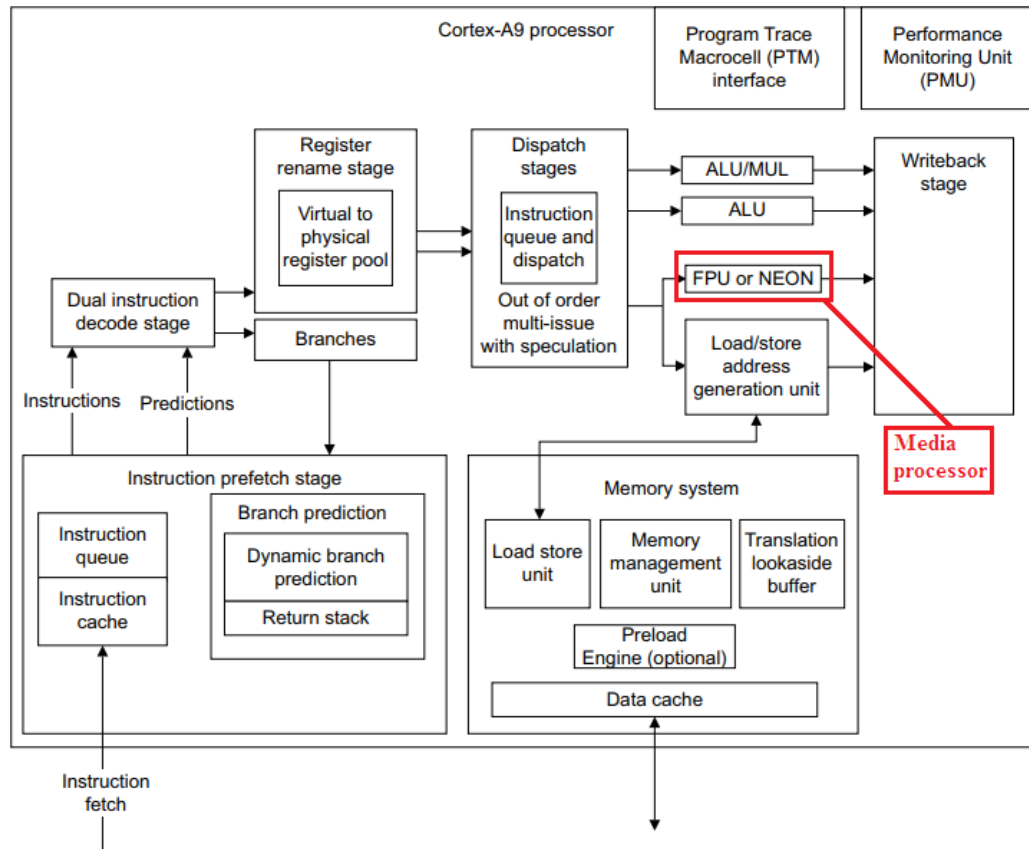
(Id.).

## EMMA Mobile EV2 Data Sheet

## BLOCK DIAGRAM



(Id.).



(E.g., [http://infocenter.arm.com/help/topic/com.arm.doc.ddi0388f/DDI0388F\\_cortex\\_a9\\_r2p2\\_trm.pdf](http://infocenter.arm.com/help/topic/com.arm.doc.ddi0388f/DDI0388F_cortex_a9_r2p2_trm.pdf)).

29. The Accused Instrumentality comprises media processors with each processor comprising a multiplier (e.g., an Integer MUL or FP MUL) having a data input coupled to the media processing unit input/output, an instruction input coupled to the media processing unit input/output, and a data output coupled to the media processing unit input/output. As shown below, the Accused Instrumentality comprises multiple ARM cortex-A9 processors, each processor comprises a NEON media coprocessor and acts as a media processing unit. NEON media coprocessor comprises a multiplier which is coupled to the inputs/outputs of the processor. Upon information and belief, the multiplier comprises a data input, an instruction input, and a data output coupled to the input/output of the processor.

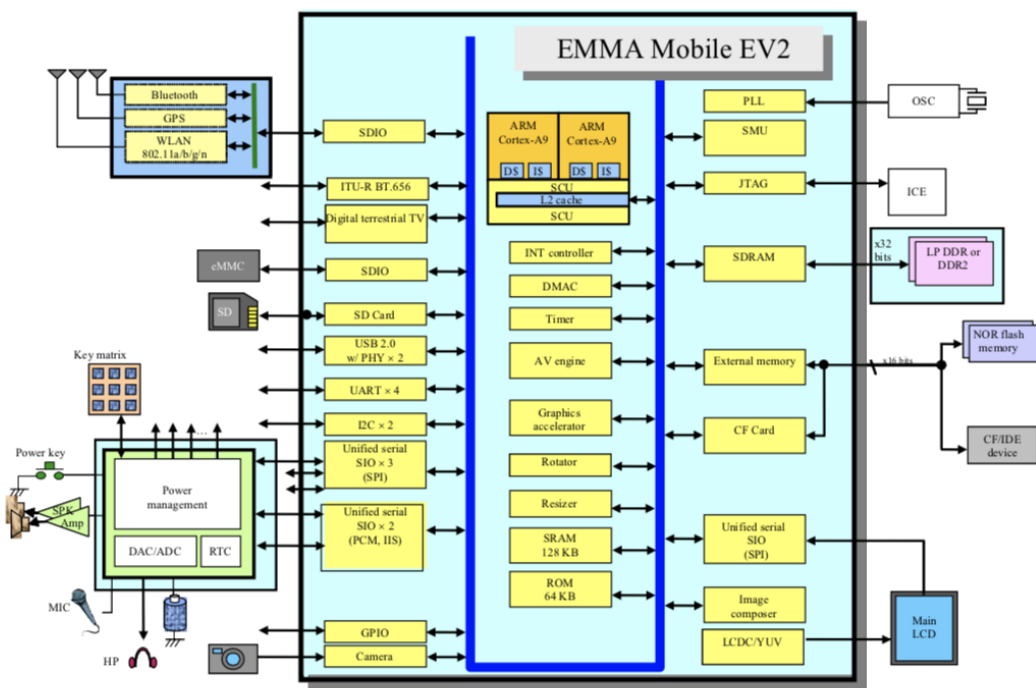
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    - I2C × 2
    - Unified serial interface × 6 (SPI, I2S)

(*E.g., id.*).

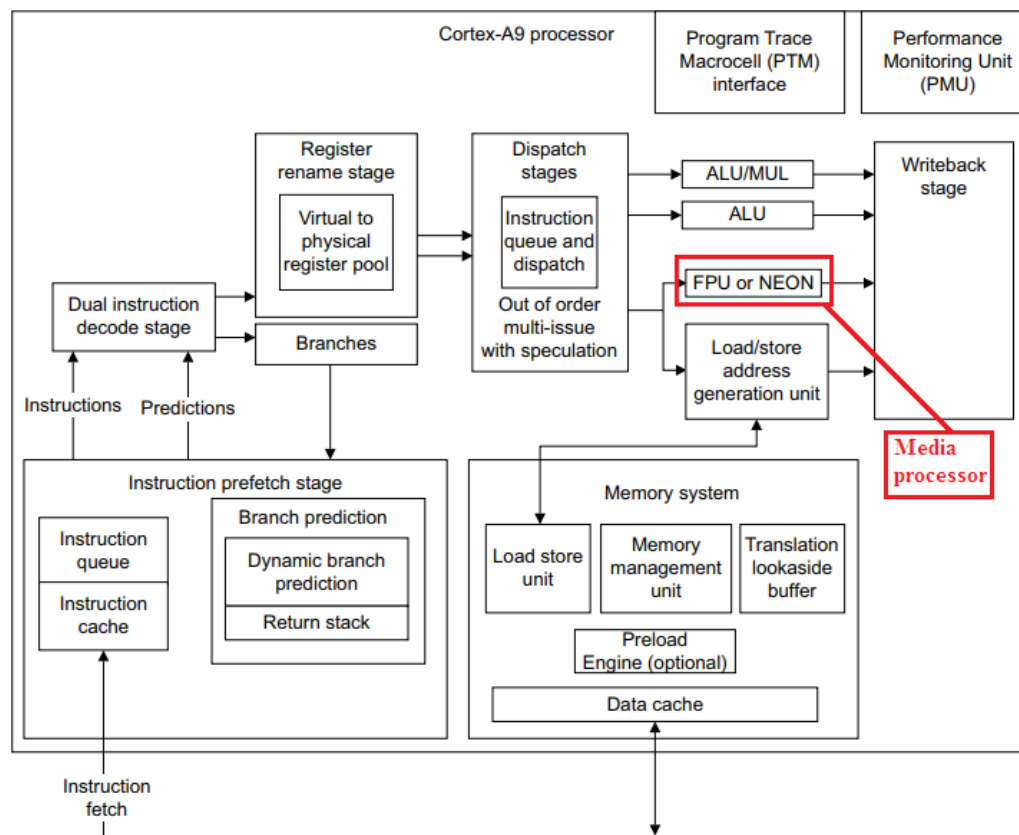
## EMMA Mobile EV2 Data Sheet

## BLOCK DIAGRAM



(Id.).





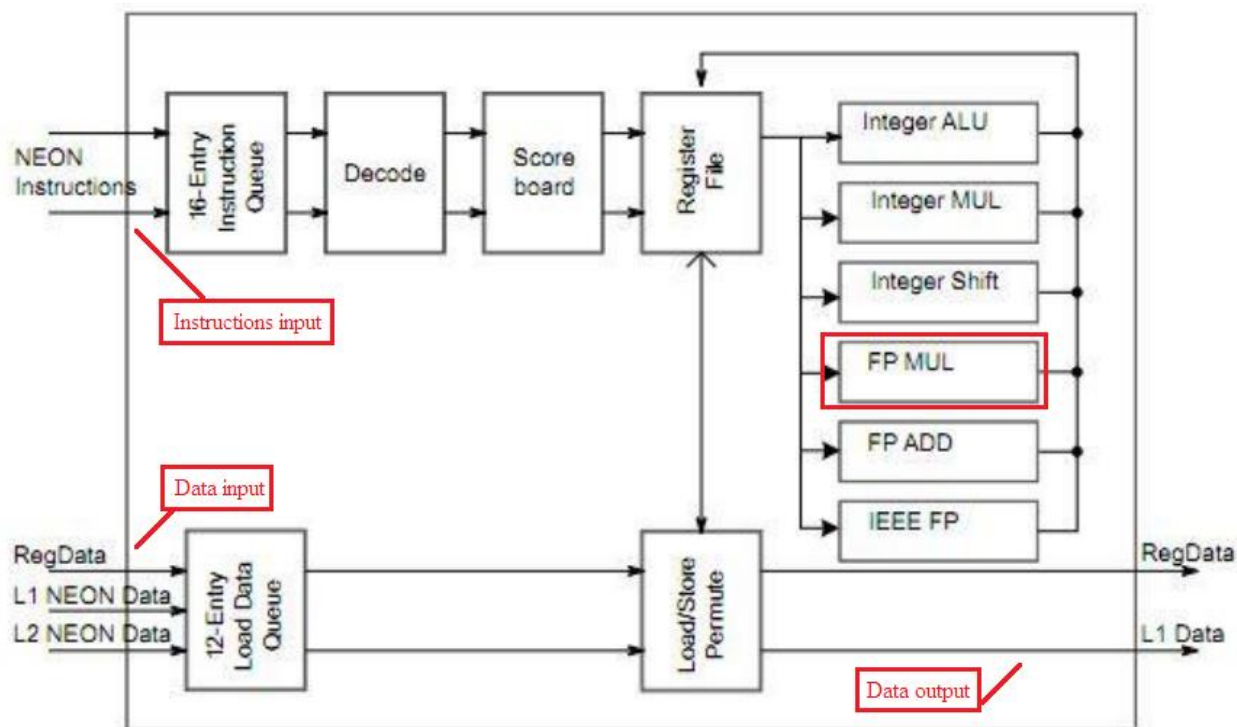
(e.g., [http://infocenter.arm.com/help/topic/com.arm.doc.ddi0388f/DDI0388F\\_cortex\\_a9\\_r2p2\\_trm.pdf](http://infocenter.arm.com/help/topic/com.arm.doc.ddi0388f/DDI0388F_cortex_a9_r2p2_trm.pdf)).

### Background

The NEON subsystem is an advanced SIMD (Single Instruction, Multiple Data) processing unit. This means that it can apply a single type of instruction to many pieces of data at one time in parallel. This is extremely helpful when it comes to media processing such as audio/video filters and codecs.

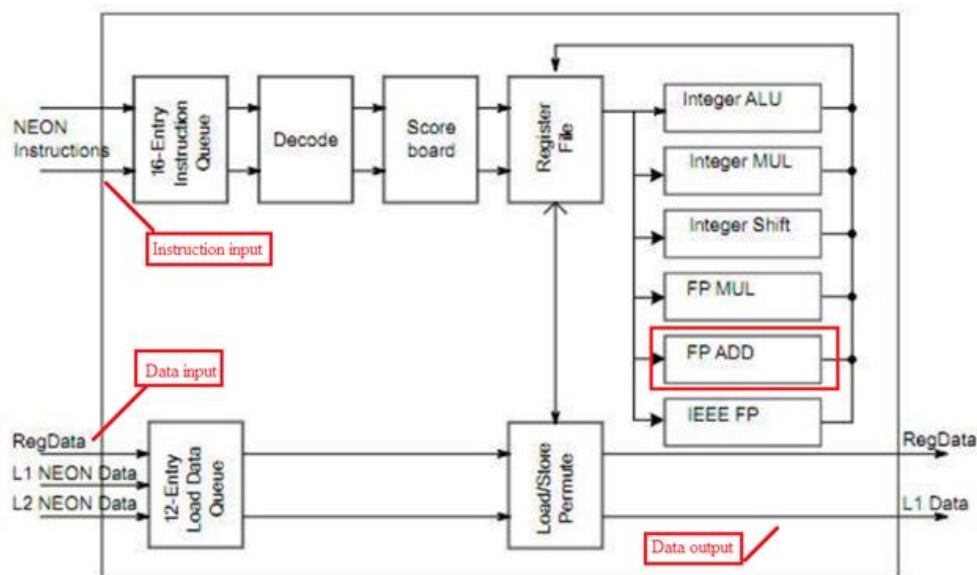
The NEON system is NOT the floating point unit of the ARM processor. There is separate FPU known as the VFP system. They use the same register space but this is taken care of by the compiler/kernel. There are a few differences between the NEON and VFP systems such as: NEON does not support double-precision floating point numbers, NEON only works on vectors and does not support advanced operations such as square root and divide.

(e.g., <http://www.add.ece.ufl.edu/4924/docs/arm/ARM%20NEON%20Development.pdf>).



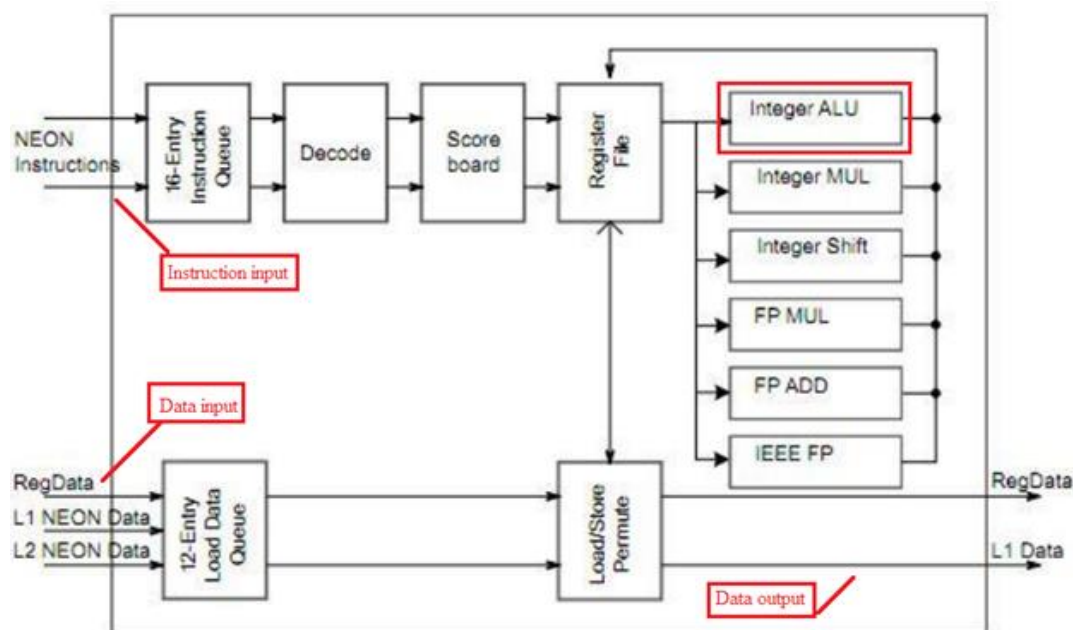
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30. The Accused Instrumentality comprises media processors with each processor comprising an arithmetic unit (e.g., an FP ADD) having a data input coupled to the media processing unit input/output, an instruction input coupled to the media processing unit input/output, and a data output coupled to the media processing unit input/output. As shown below, the Accused Instrumentality comprises multiple ARM cortex-A9 processor, each processor comprises a NEON media coprocessor and acts as a media processing unit. NEON media coprocessor comprises an arithmetic unit which is coupled to the inputs/outputs of the processor. Upon information and belief, the arithmetic unit comprises a data input, an instruction input, and a data output coupled to the input/output of the processor.



(E.g., <http://www.add.ece.ufl.edu/4924/docs/arm/ARM%20NEON%20Development.pdf>).

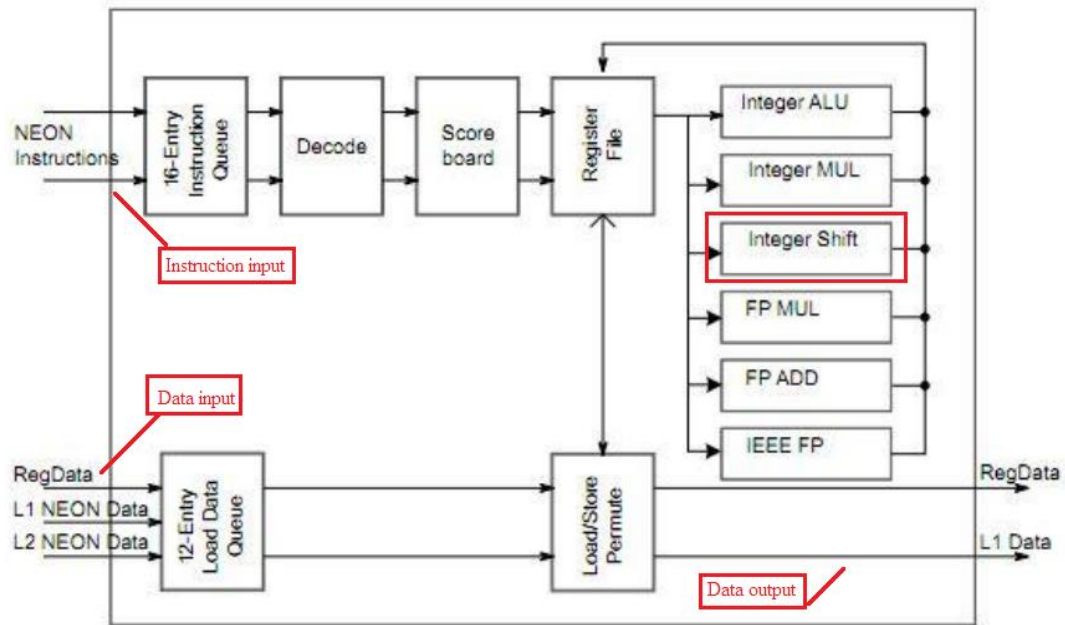
31. The Accused Instrumentality comprises media processors with each processor comprising an arithmetic logic unit (e.g., an ALU) having a data input coupled to the media processing unit input/output, an instruction input coupled to the media processing unit input/output, and a data output coupled to the media processing unit input/output, capable of operating concurrently with at least one selected from the multiplier (e.g., an Integer MUL or FP MUL) and arithmetic unit (e.g., a FP ADD). As shown below, the Accused Instrumentality comprises multiple ARM cortex-A9 processor, each processor comprises a NEON media coprocessor and acts as a media processing unit. NEON media coprocessor comprises an arithmetic logical unit which is coupled to the inputs/outputs of the processor. Upon information and belief, the arithmetic logical unit comprises a data input, an instruction input, and a data output coupled to the input/output of the processor. Upon information and belief, the arithmetic logical unit (e.g., the Integer ALU) is capable of operating concurrently with at least one selected from the multiplier (e.g., the Integer MUL or FP MUL) and arithmetic unit (e.g., the FP ADD).



(E.g., <http://www.add.ece.ufl.edu/4924/docs/arm/ARM%20NEON%20Development.pdf>).

32. The Accused Instrumentality comprises media processors with each processor comprising a bit manipulation unit (e.g., an Integer Shift unit) having a data input coupled to the media processing unit input/output, an instruction input coupled to the media processing unit input/output, and a data output coupled to the media processing unit input/output, capable of operating concurrently with the arithmetic logic unit (e.g., an Integer ALU) and at least one selected from the multiplier (e.g., an Integer MUL or FP MUL) and arithmetic unit (e.g., a FP ADD). As shown below, the Accused Instrumentality comprises multiple ARM cortex-A9 processors, each processor comprising a NEON media coprocessor that acts as a media processing unit. The NEON media coprocessor comprises an integer shift unit (i.e., bit manipulation unit) which is coupled to the inputs/outputs of the processor. Upon information and belief, the integer shift unit (i.e., bit manipulation unit) comprises a data input, an instruction input, and a data output coupled to the input/output of the processor. Upon information and belief, the integer shift unit (i.e., bit manipulation unit) is capable of operating concurrently with

the arithmetic logic unit (*e.g.*, the Integer ALU) and at least one selected from the multiplier (*e.g.*, the Integer MUL or FP MUL) and arithmetic unit (*e.g.*, the FP ADD).



(*E.g.*, <http://www.add.ece.ufl.edu/4924/docs/arm/ARM%20NEON%20Development.pdf>).

33. The Accused Instrumentality comprises a plurality of media processors (*e.g.*, ARM cortex-A9 processors) for performing at least one operation, simultaneously with the performance of other operations by other media processing units (*e.g.*, another ARM cortex-A9 processor on the same chip).

**FEATURES**

- CPU: ARM Cortex-A9 (Frequency: 533 MHz, I-cache: 32 KB, D-cache: 32 KB, L2 cache : 256KB)
- AV engine: High-performance multimedia processor
  - Video:
    - Decoder: Multi decoder (H.264, VC-1, MPEG 1/2, H.263, MPEG-4: up to 1080p 30fps), other decoders/encoders may be implemented by software using CPU resources
  - Audio:
    - Decoder: MPEG-4 HE-AAC decoder, enhanced aacPlus decoder
- 3D Graphics accelerator (A3D)
  - 3D: 14.7 Mpix/sec
  - Supporting Open-GL-ES2.0, OpenGL-ES1.x
- Image processor: Resizing, rotating, image composing with alpha blending and key color masking
- Image composer: Image composing with alpha blending and key color masking, gamma correction
  - Direct connection to LCD interface
- Security functions: Secure boot function, secure timer, secure watchdog timer, secure DMA
- Internal memories: SRAM: 128 KB, ROM: 64 KB
- DMA controller: 8 channels
- Timers: Interval timers and watchdog timers: 15 channels
- DRAM interface:
  - LPDDR-SDRAM interface: Max 200 MHz DDR (DDR400), 32 bits, up to 1.6 GB/s
  - DDR2-SDRAM interface: Max 266 MHz DDR (DDR533), 32 bits, up to 2.1 GB/s
- NOR-Flash interface: 16-bit data bus
- Peripheral interfaces:
  - Memory card interface: SD card (with CPRM<sup>Note</sup>) × 1, SDIO × 3, CF card interface (Note : Option)
  - Image interfaces:
    - LCD interface → Parallel interface
    - ITU-R BT.656 interface
    - Camera interface → Parallel interface
  - Other serial interfaces:
    - USB 2.0 host × 1 and peripheral × 1 (with PHY)
    - UART × 4
    - I2C × 2
    - Unified serial interface × 6 (SPI, I2S)

(e.g., [https://www.renesas.com/us/en/doc/DocumentServer/030/r19ds0010ej1200\\_ds.pdf](https://www.renesas.com/us/en/doc/DocumentServer/030/r19ds0010ej1200_ds.pdf)).

**Background**

The NEON subsystem is an advanced SIMD (Single Instruction, Multiple Data) processing unit. This means that it can apply a single type of instruction to many pieces of data at one time in parallel. This is extremely helpful when it comes to media processing such as audio/video filters and codecs.

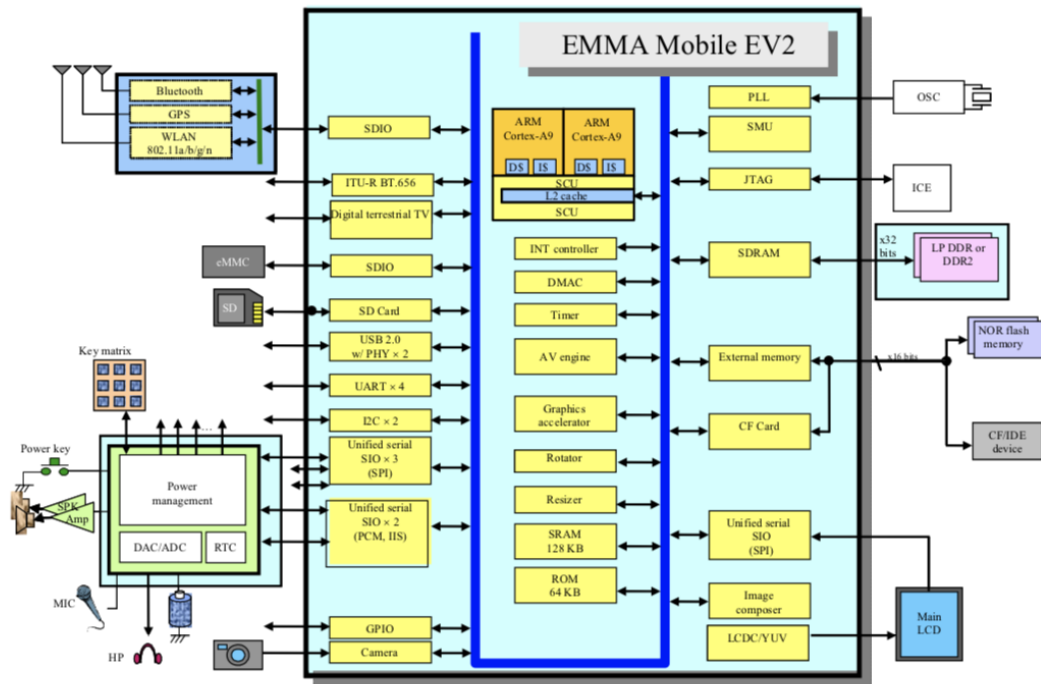
The NEON system is NOT the floating point unit of the ARM processor. There is separate FPU known as the VFP system. They use the same register space but this is taken care of by the compiler/kernel. There are a few differences between the NEON and VFP systems such as: NEON does not support double-precision floating point numbers, NEON only works on vectors and does not support advanced operations such as square root and divide.

(E.g., <http://www.add.ece.ufl.edu/4924/docs/arm/ARM%20NEON%20Development.pdf>).

34. The Accused Instrumentality comprises a plurality of media processors (e.g., ARM cortex-A9 processors), each processor receiving at the media processor input/output an instruction and data from the memory, and processing the data responsive to the instruction received to produce at least one result. As shown below, each ARM cortex-A9 processor comprises a NEON media coprocessor which receives instructions and data from memory and processes the data responsive to the instruction received in order to produce a result.

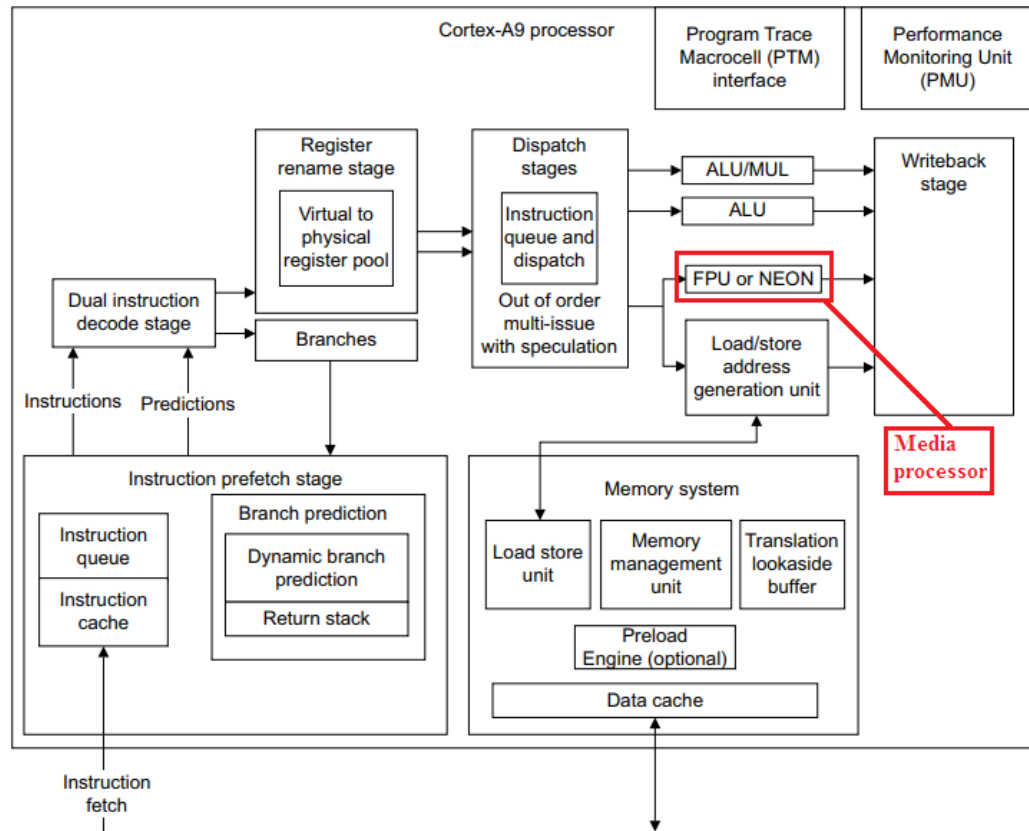
#### EMMA Mobile EV2 Data Sheet

#### BLOCK DIAGRAM

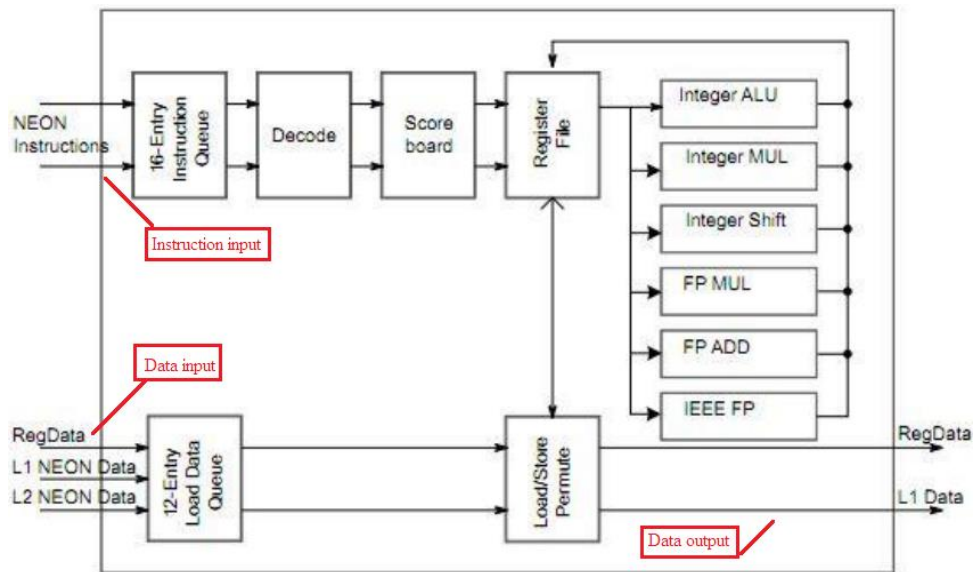


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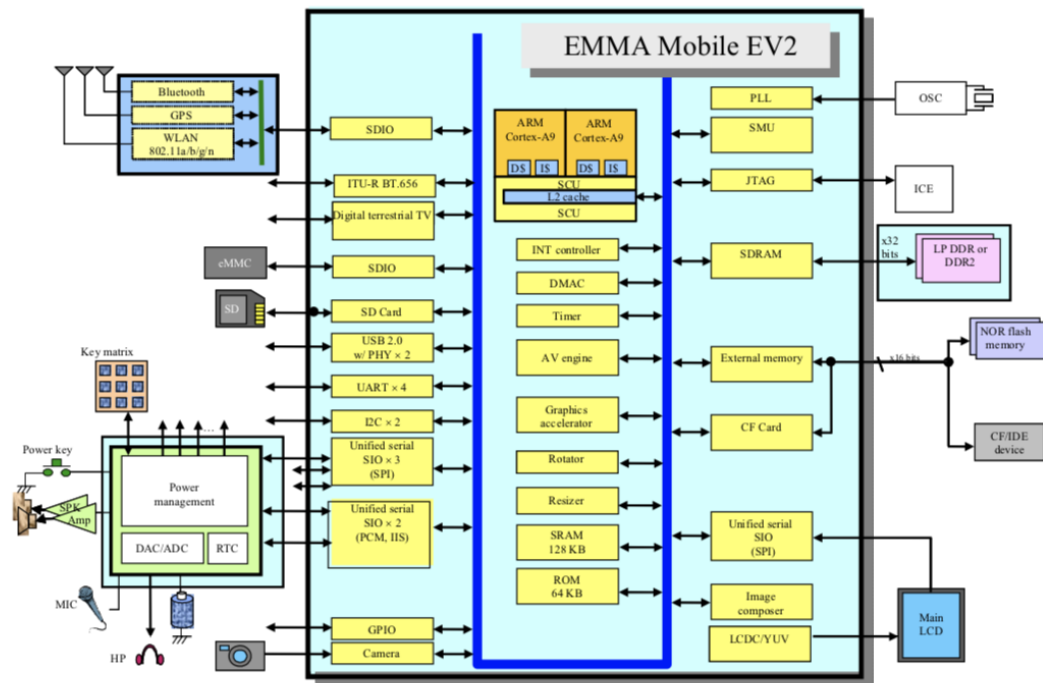
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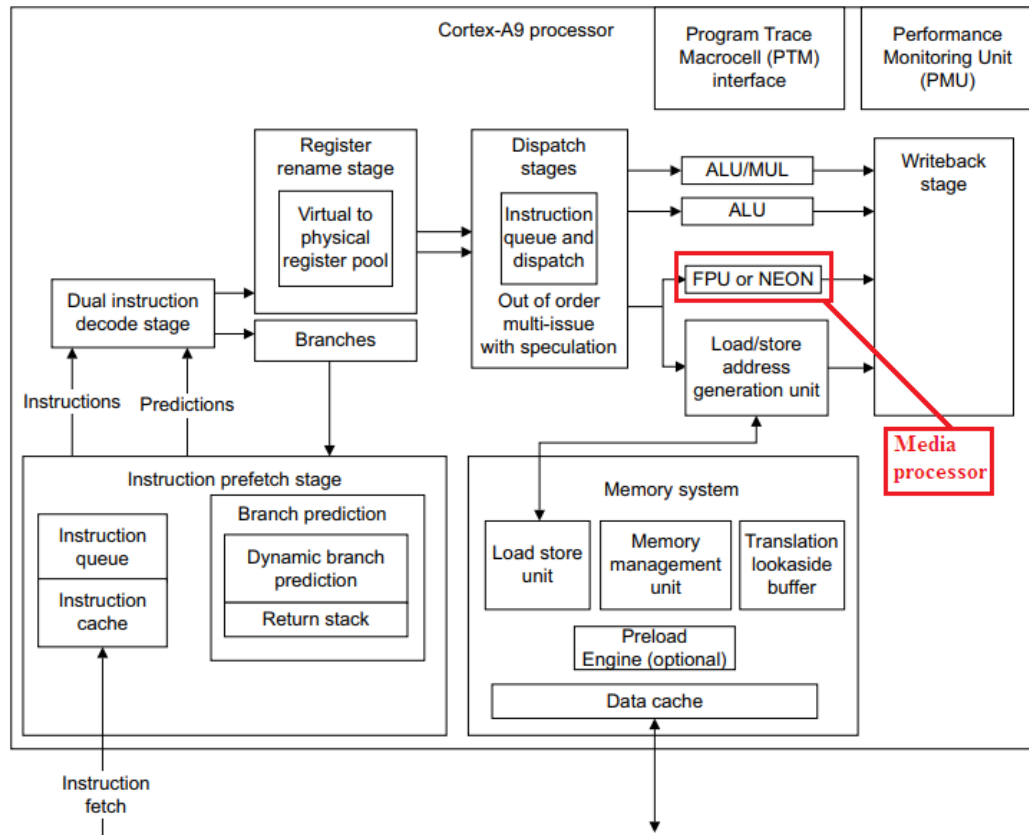
35. The Accused Instrumentality comprises a plurality of media processors (e.g., ARM cortex-A9 processors), each processor providing at least one of the at least one result at the media processor input/output. (*Supra* ¶34).

#### EMMA Mobile EV2 Data Sheet

#### BLOCK DIAGRAM

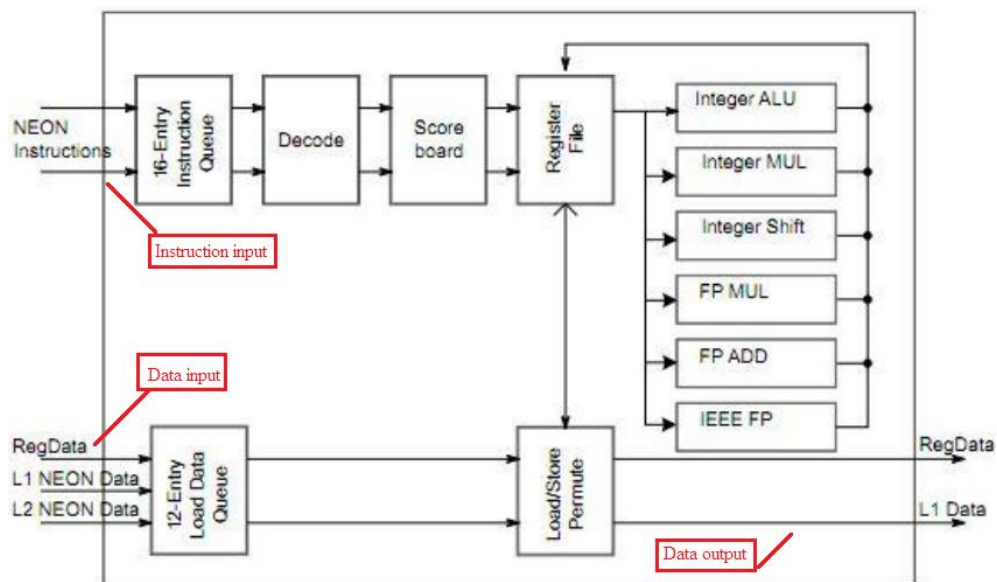


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1 July 30, 2019

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**JURY DEMAND**

Plaintiff, under Rule 38 of the Federal Rules of Civil Procedure, requests a trial by jury of any issues so triable by right.

July 30, 2019

By /s/Steven A. Nielsen

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be filed)  
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